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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/633,544	08/05/2003	Noriaki Saito	030883	6424

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EXAMINER	
MONDT, JOHANNES P	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 02/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/633,544	SAITO ET AL.	
	Examiner	Art Unit	
	Johannes P. Mondt	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) *11-21* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *8/5/03* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/17/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. ***Claims 11-21*** have been withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Group and/or Species, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 01/13/2005.

Information Disclosure Statement

The examiner has considered the items listed on the Information Disclosure Statement filed 08/17/2004. A signed copy of Form PTO-1449 is herewith enclosed.

Drawings

2. ***Figures 1, 2 and 3*** should be designated by a legend such as ***--Prior Art--*** because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. ***Claims 1- 2, 5- 6, 9 and 10*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art as Admitted by Applicant in view of Osada et al (6,066,916). Prior Art as Admitted by Applicant teaches (Figures 1-3 and paragraphs [0001]-0010] and [0014]-[0016]) a semiconductor device comprising:

a protective circuit ([0008]) including a plurality of protective elements (PMOS Transistors PT1, PT2, ..., Pn, NMOS Transistors NT1, Nt2, ..., NTn, and two sets of parallel resistors 4 and 5; cf. paragraphs [0007]-[0008]) connected in parallel between a signal line 3 ([0007]) and a power supply line (line between relatively high voltage V_{DD} and relative low voltage V_{SS}: cf. [0007]), each including a plurality of metal oxide semiconductor (MOS) transistors (PT1, ..., PTn, NT1, ..., NTn) (cf. [0007]-[0008]), and a plurality of resistors 4 and 5 (loc.cit.), wherein, in the respective protective elements, drains of the MOS transistors are connected to the signal line 3 that establishes a connection between a pad and an internal circuit through the resistors (4 to the side of V_{DD}, and 5 to the side of V_{SS}: Figure 1 and [0007]), and source of the MOS transistors (all NTn and PTn) are connected to the power supply line (the sources, by default, are

those terminals of the transistors not connected to the resistors and instead, as shown by Figure 1, connected to the power supply line, because the drains are indeed connected to the resistors 4 and 5: see [0007] and [0008]).

Prior Art as Admitted by Applicant does not necessarily teach the limitation on resistance of the resistors as claimed. However, said limitation merely applies what is well known in the art of parallel arrays of devices requiring, - or at least preferentially having, the same voltage level, i.e., the same overall wiring resistance between their terminals: in particular, it would have been obvious to include said limitation in view of Osada et al, who, in a parallel array of device components (in this case data electrodes 2; see title, abstract, and "Field of Invention") requiring or at least preferentially having the same wiring resistance between their terminals 21, teach to compensate for the different parasitic resistances (wiring lead resistances of wires 2b and 2c) by connecting additional resistors (compensating resistors 10) so as to achieve the same overall wiring resistance (col. 2, l. 30-41, col. 3, l. 18-53 and col. 5, l. 46-57; see Figure 7).

Straightforward application to the Prior Art as Admitted by Applicant results in a gradually decreased resistance of said resistors 4 and 5 from the pad toward the internal circuit, because the parasitic resistance of those resistance paths increases toward the internal circuit.

Motivation for inclusion of the teaching by Osada et al in the invention of the Prior Art as Admitted by Applicant derives from the stated values of the overall resistance as equal to a fixed resistance r augmented by a parasitic resistance increasing with connecting wire length along the signal line 3 (Specification, paragraph [0009] and the

nature of "parasitic" as being unwanted, while the resulting unequal wiring resistances is exactly what Osada et al solve.

On claim 2: the resistance of the resistors becomes lower from the pad toward the internal circuit according to a parasitic resistance of the signal line in the combined invention, because the parasitic resistance for which the compensating resistors 10 provide compensation increases toward the internal circuit in the Prior Art as Admitted by Applicant.

On claims 5 and 6: Prior Art as Admitted by Applicant teaches the resistors to be silicide blocks 7 and 9 (thus meeting claim 6) formed on the drain side of the transistors, hence to be silicide resistors (meeting a forteriori claim 5) formed on a semiconductor substrate.

On claim 9: the resistors are elements each formed with a combination of at least two selected from a group consisting of polysilicon resistors, well resistors, silicide resistors and silicide blocks, because the silicide blocks in the Prior Art as admitted by Applicant are both silicide resistors and silicide blocks.

On claim 10: implementation of the teaching by Osada et al implies correction for the parasitic resistance of the lead or wire, and because said parasitic resistance goes up with increasing wire or lead length the resistance of the resistors in each of the protective elements is gradually decreased from the previous one among the resistors from the pad toward the internal circuit.

5. ***Claims 3-4*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art as Admitted by Applicant and Osada et al as applied to claim 1 above, and further in

view of Longcor et al (4,987,465). *As detailed above, claim 1 is unpatentable over Prior Art as Admitted by Applicant in view of Osada et al. Neither Prior Art as Admitted by Applicant nor Osada et al necessarily teach the further limitation as defined by claim 3 nor that of claim 4. However, Prior Art as Admitted by Applicant does teach the resistors to be resistors formed on a semiconductor substrate, while it would have been obvious to include said further limitation in view of Longcor et al,* who teach *polysilicon* for the substrate material in CMOS technology for ESD protection with adjustable dropping resistance (resistance in the polysilicon substrate) (title, abstract and col. 3, l. 43-56), thus meeting claim 3, and, furthermore, in a preferred embodiment, in an n-well region (col. 3, l. 52-54), thus meeting claim 4. *Motivation* to include the teaching by Longcor et al in the combined invention, in addition to the cost saving of using polysilicon rather than crystalline silicon, at least derives from the well known use of polysilicon for the purpose of CMOS substrate for ESD protection devices with adjustable substrate resistance value and the circumstance that CMOS technology is indeed taught by the Prior Art as Admitted by Applicant to be the basis for the invention (cf. also Specification, paragraph [0005]). Applicant is reminded in this regard that it has been held that mere selection of known materials generally understood to be suitable to make a device, the selection of the particular material being on the basis of suitability for the intended use, would be entirely obvious. *In re Leshin 125 USPQ 416.*

6. ***Claims 7-8*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art as Admitted by Applicant as applied to claim 1 above, and further in view of Hsu et al (6,153,913). *As detailed above, claim 1 is unpatentable over Prior Art as Admitted by*

Applicant in view of Osada et al. Neither necessarily teach the further limitation as defined by claim 7 nor the further limitation as defined by claim 8.

However, it would have been obvious to include said further limitation as defined by claim 7 in view of Hsu et al, who, in a patent on a more uniformly distributed ESD current in MOS ESD protection devices (title, abstract and col. 2, l. 32-59), hence analogous art, teach that the silicide blocks 140 (col. 4, l. 13) , i.e., the elements as claimed as admitted as Prior Art by Applicant, are evenly distributed within the drain region 122 (abstract and col. 4, l. 5) so as to promote even distribution of the ESD transient current (col. 2, l. 47-60). Because said silicide blocks are regions of relatively low electrical resistivity (col. 3, l. 46-47) positioned in the drain region they are part of the drain wiring while inherently having a resistance that depends on their length and their width: changing either their length or their width thus inherently results in a change in their resistance and said change is thus imparted by changing at least one of a length and a width of said drain wiring. *Motivation* to include the teaching by Hsu et al in the invention of the Prior Art as Admitted by Applicant derives from the resulting uniform distribution of the ESD current, thus improving the functionality of the ESD protection circuit (col. 2, l. 53-59).

On claim 8: it would have been obvious to include the further limitation as defined by claim 8 in view of Hsu et al, according to whom the silicide blocks discussed above (discussion of claim 7) are the elements with which the resistors are formed and whose resistance is changed by changing a number of contacts that establish electric connections between drain wirings 130 (col. 4, l. 5) connected to the signal line, said

number of contacts 130 (see Figure 5) clearly being variable and inherently changing by their variation in number the resistance of the drain wiring, given that resistance of a wiring goes down with the number of parallel current paths. Motivation to include the teaching by Hsu et al in this regard in the invention of the Prior Art as Admitted by Applicant derives from the resulting improvement of the ESD current distribution.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JPM
February 21, 2005

Patent Examiner:
Johannes Mondt (Art Unit: 2826)